

Docket No.: 071971-0015



PATENT

TFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277  
Shiro SAKIYAMA, et al. : Confirmation Number: CNF NO. 6689  
Application No.: 10/511,165 : Group Art Unit: 2816  
Filed: October 14, 2004 : Examiner: HILTUNEN, THOMAS J  
For: SEMICONDUCTOR INTEGRATED CIRCUIT

**SECOND REQUEST FOR CORRECTED FILING RECEIPT**

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P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that the Domestic priority data is incorrect. Attached is a copy of the Front Page of the Published International Application, which evidences that the Domestic Priority data should read: PCT/JP04/01942 02/19/2004. It is requested that a corrected filing receipt be issued.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

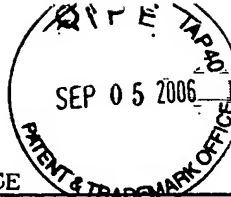
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/511,165	10/14/2004	2811	1250	71971-015	18	16	3

CONFIRMATION NO. 6689

20277  
 MCDERMOTT WILL & EMERY LLP  
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 WASHINGTON, DC 20005-3096

## FILING RECEIPT



\*OC000000015503501\*

Date Mailed: 04/08/2005

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

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Power of Attorney: The patent practitioners associated with Customer Number 20277.

## Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP04/01942 02/19/2003

02/19/2004

## Foreign Applications

JAPAN 2003-047418 02/25/2003

Projected Publication Date: To Be Determined - pending completion of Security Review

Non-Publication Request: No

Early Publication Request: No

## Title

Semiconductor integrated circuit

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APR 13 2005

MCDERMOTT, WILL &amp; EMERY

Preliminary Class

257

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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(12)特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関  
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(43) 国際公開日  
2004年9月10日 (10.09.2004)

PCT

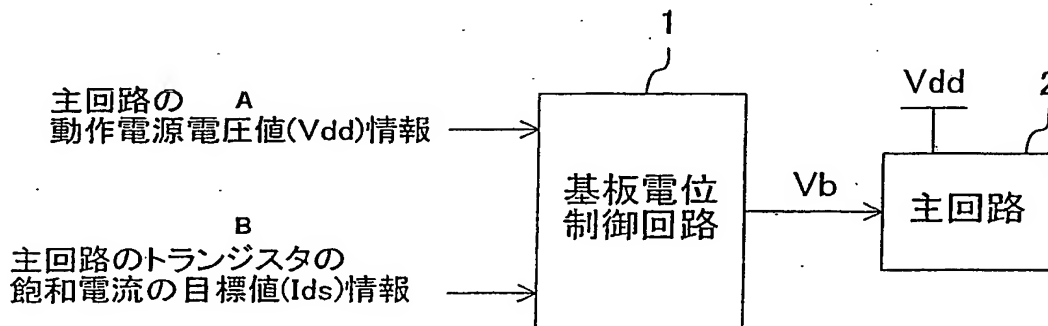
(10) 国際公開番号  
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- (51) 国際特許分類<sup>7</sup>: H03K 17/687, 19/094, H01L 27/088 (74) 代理人: 前田 弘, 外(MAEDA, Hiroshi et al.); 〒5500004 大阪府大阪市西区靱本町1丁目4番8号本町中島ビル Osaka (JP).
- (21) 国際出願番号: PCT/JP2004/001942
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- (30) 優先権データ:  
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- (81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
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- (84) 指定国 (表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU,

[続葉有]

(54) Title: SEMICONDUCTOR INTEGRATED CIRCUIT

(54) 発明の名称: 半導体集積回路



A...INFORMATION CONCERNING OPERATING POWER  
SUPPLY VOLTAGE (Vdd) OF MAIN CIRCUIT  
B...INFORMATION CONCERNING TARGET SATURATION  
CURRENT VALUE (IdS) OF TRANSISTOR OF MAIN CIRCUIT  
1...SUBSTRATE POTENTIAL CONTROLLING CIRCUIT  
2...MAIN CIRCUIT

(57) Abstract: A semiconductor integrated circuit comprises a main circuit (2) which is composed of a MOS transistor wherein a source and a substrate are separated from each other. A substrate potential controlling circuit (1) controls the substrate potential of the MOS transistor of the main circuit (2) so that the actual saturation current value of the MOS transistor which constitutes the main circuit (2) becomes equal to a target saturation current value (IdS) of the main circuit (2) at the operating power supply voltage (Vdd). Consequently, even when the operating power supply voltage of the semiconductor integrated circuit is lowered, variations in the operating speed can be suppressed within a small range.

[続葉有]

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